Claims

[c1] 1. A chip package structure, comprising: a carrier having at least one signal contact, a pair of first non-signal contacts and a pair of second non-signal contacts, wherein the signal contact, the pair of first non-signal contacts and the pair of second non-signal contacts are positioned on the surface of the carrier, and the second non-signal contacts are electrically connected to each other; a die having an active surface and a corresponding back surface, wherein the back surface of the die is attached to one surface of the carrier, the die further includes a signal pad, a pair of first non-signal pads and a pair of second non-signal pads, the signal pad, the pair of first non-signal pads and the pair of second non-signal pads are positioned on the active surface of the die, and furthermore, the pair of second non-signal contacts is closer to the die than the signal contact or the pair of first non-signal contacts; a signal wire whose ends are connected to the signal pad and the signal contact respectively; a pair of first non-signal wires, wherein the two ends of each first non-signal wire are connected to one of the first non-signal pads and one of the first non-signal contacts respectively, and the first non-signal wires of the first non-signal wire pair are on each side of the signal wire; and a pair of second non-signal wires, wherein the two ends of the each second non-signal wire are connected to one of the second non-signal pads and one of the second non-signal contacts respectively, and the second non-signal wires of the second non-signal wire pair are on each side of the signal wire and first non-signal wire pair assembly.

[c2] 2. The chip package structure of claim 1, wherein the package further includes a molding compound that encapsulates the die, the signal wire, the pair of first non-signal wires and the pair of second non-signal wires.

[c3] 3. The chip package structure of claim 1, wherein the pair of first non-signal contacts are ground contacts, the pair of first non-signal pads are ground pads and the pair of first non-signal wires are ground wires.

[c4] 4. The chip package structure of claim 1, wherein the pair of first non-signal contacts are power contacts, the pair of first non-signal pads are power pads

and the pair of first non-signal wires are power wires.

[c5] 5. The chip package structure of claim 1, wherein the pair of second non-signal contacts are ground contacts, the pair of second non-signal pads are ground pads and the pair of second non-signal wires are ground wires.

[c6] 6. The chip package structure of claim 5, wherein the carrier further includes a ground ring on the surface of the carrier and a portion of the ground ring constitutes the pair of second non-signal contacts.

[c7] 7. The chip package structure of claim 1, wherein the pair of second non-signal contacts are power contacts, the pair of second non-signal pads are power pads and the pair of second non-signal wires are power wires.

[c8] 8. The chip package structure of claim 7, wherein the carrier further includes a power ring on the surface of the carrier and a portion of the power ring constitutes the pair of second non-signal contacts.

[c9] 9. The chip package structure of claim 1, wherein the carrier further includes a die pad and a plurality of electrode bumps, the electrode bumps surround the die pad, the die is attached to the upper surface of the die pad, the upper surface of the die pad constitutes the second non-signal contacts and the upper surface of a portion of the electrode bumps constitutes the signal contact and the pair of first non-signal contacts respectively.

[c10] 10. The chip package structure of claim 9, wherein the package further includes a molding compound that encapsulates the die, the signal wire, the pair of first non-signal wires and the pair of second non-signal wires.

[c11] 11. The chip package structure of claim 1, wherein the carrier further includes a chip carrier structure and a plurality of cavity conductive structures surrounding the chip carrier structure, the die is attached to the upper surface of the chip carrier structure, the upper surface of the chip carrier structure constitutes the second non-signal contacts, and the interior surface of a portion of the cavity conductive structures constitutes the signal contact and the pair of first non-signal contacts.

[c12] 12. The chip package structure of claim 11, wherein the package further includes a molding compound that encapsulates the die, the signal wire, the pair of first non-signal wires and the pair of second non-signal wires and fills the space enclosed by the interior surface of the cavity conductive structures.

[c13] 13. A chip package structure, comprising: a carrier having a plurality of first contacts and a plurality of second contacts, wherein the first contacts and the second contacts are positioned on the one surface of the carrier; a die having an active surface and a corresponding back surface, wherein the back surface of the die is attached to the surface of the carrier, the die further includes a plurality of bonding pads all positioned on the active surface of the die, and furthermore, the second contacts are closer to the die than the first contacts; a signal wire whose ends are connected to one of the bonding pads and one of the first contacts respectively; a pair of first non-signal wires, wherein the two ends of each first non-signal wire are connected to one of the bonding pads and one of the first contacts respectively, and the first non-signal wires of the first non-signal wire pair are positioned on each side of the signal wire; and a pair of second non-signal wires, wherein the two ends of the each second non-signal wire are connected to one of the bonding pads and one of second contacts respectively, and the second non-signal wires of the second non-signal wire pair are on each side of the signal wire and first non-signal wire pair assembly.

[c14] 14. The chip package structure of claim 13, wherein the package further includes a molding compound that encapsulates the die, the signal wire, the pair of first non-signal wires and the pair of second non-signal wires.

[c15] 15. The chip package structure of claim 13, wherein the pair of first non-signal wires are ground wires.

[c16] 16. The chip package structure of claim 13, wherein the pair of first non-signal wires are power wires.

[c17] 17. The chip package structure of claim 13, wherein the pair of second non-signal wires are ground wires.

[c18] 18. The chip package structure of claim 17, wherein the carrier further includes a ground ring on the surface of the carrier and a portion of the ground ring constitutes the second contacts.

[c19] 19. The chip package structure of claim 13, wherein the pair of second non-signal wires are power wires.

[c20] 20. The chip package structure of claim 19, wherein the carrier further includes a power ring on the surface of the carrier and a portion of the power ring constitutes the second contacts.

[c21] 21. The chip package structure of claim 13, wherein the carrier includes a die and a plurality of electrode bumps that surrounds the die pad, the die is attached to the upper surface of the die pad, the upper surface of the die pad constitutes the second contacts and the upper surface of a portion of the electrode bumps constitutes the first contacts.

[c22] 22. The chip package structure of claim 21, wherein the package further includes a molding compound that encapsulates the die, the signal wire, the pair of first non-signal wires and the pair of second non-signal wires.

[c23] 23. The chip package structure of claim 13, wherein the carrier includes a chip carrier structure and a plurality of cavity conductive structures surrounding the chip carrier structure, the die is attached to the upper surface of the chip carrier structure, the upper surface of the chip carrier structure constitutes the second non-signal contacts, and the interior surface of a portion of the cavity conductive structures constitutes the first contacts.

[c24] 24. The chip package structure of claim 13, wherein the package further includes a molding compound that encapsulates the die, the signal wire, the pair of first non-signal wires and the pair of second non-signal wires and fills the space enclosed by the interior surface of the cavity conductive structures.